

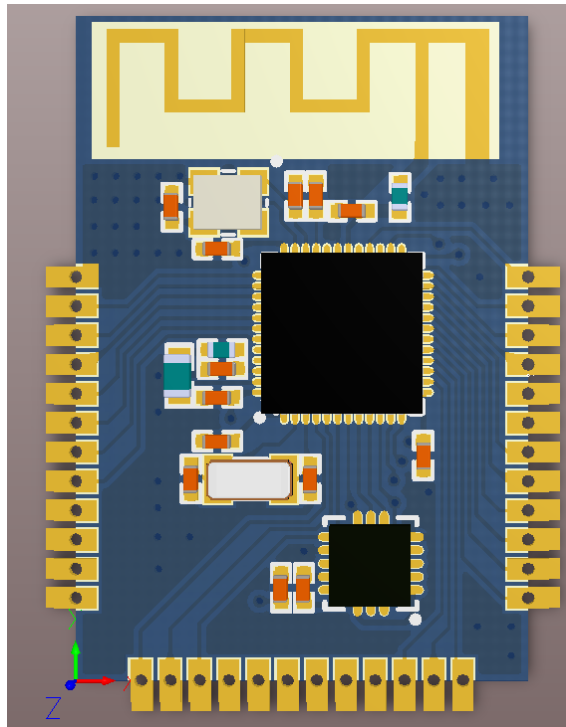
MK04 series BLE Module Datasheet

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1. Product Description

MK04 series module is a highly integrated BLE[®] 4.2 module with NFC function, it was designed for high data rate, short-range wireless communication in the 2.4GHz ISM band. The module is designed based on Nordic[®] Semiconductor nRF52832 radio Transceiver IC, has a 32 bit ARM[®] Cortex-M4 CPU, flash memory and analog and digital peripherals. MK04 provides a low power and ultra-low cost BLE and proprietary protocols for wireless transmission applications.



2. Product Classification

Product Model	Sensor
MK04A	NONE
MK04B	LIS3DH

3. Key Features

- 32 bits ARM® Cortexm-M4 @ 16MHz
- 2.4GHz multi-protocol transceiver
- -96 dBm sensitivity in Bluetooth® low energy mode
- 64kB RAM
- 512kB Flash
- 5.3 mA peak current in TX (0 dBm)
- 5.4 mA peak current in RX
- 29 configurable I/O pins
- Programmable peripheral interconnect (PPI)
- AES HW encryption with EasyDMA
- RNG, RTC
- Temperature sensor
- Up to 3x SPI master/slave with EasyDMA
- Up to 2x I2C compatible 2-Wire master/slave
- I2S with EasyDMA
- UART (CTS/RTS) with EasyDMA
- 3x 4-channel pulse width modulator (PWM) units with EasyDMA
- Digital microphone interface (PDM)
- 5x 32-bit timers with counter mode
- Quadrature decoder (QDEC)
- 12-bit, 200 kbps ADC - 8 configurable channels with programmable gain
- 64 level comparator
- Single-pin antenna interface
- NFC-A tag

- Tx Power -20 to +4 dBm in 4 dB steps
- Supply voltage range : 1.7V to 3.6V
- Dimension :25x17x1.0mm

4. Applications

Internet of Things (IoT)

- Home automation
- Sensor networks
- Building automation
- Industrial
- Retail

Personal area networks

- Health/fitness sensor and monitor devices
- Medical devices
- Key fobs and wrist watches

Interactive entertainment devices

- Remote controls
- Gaming controllers

Beacons

A4WP wireless chargers and devices

Remote control toys

Computer peripherals and I/O devices

- Mouse
- Keyboard
- Multi-touch trackpad
- Gaming

5. Interfaces

5.1 Power Supply

Regulated power for the **MK04** is required. The input voltage VCC range should be 1.7V to 3.6V. Suitable decoupling must be provided by external decoupling circuitry (10uF and 0.1uF). It can reduce the noise from power supply and increase power stability.

5.2 System Function Interfaces

5.2.1 GPIOs

The general purpose I/O is organized as one port with up to 21 I/Os enabling access and control of up to 21 pins through one port. Each GPIO can be accessed individually with the following user configurable features:

- ◆ Input/output direction
- ◆ Output drive strength
- ◆ Internal pull-up and pull-down resistors
- ◆ Wake-up from high or low level triggers on all pins

- ◆ Trigger interrupt on all pins
- ◆ All pins can be used by the PPI task/event system; the maximum number of pins that can be interfaced through the PPI at the same time is limited by the number of GPIOTE channels
- ◆ All pins can be individually configured to carry serial interface or quadrature demodulator signals
- ◆ All pins can be configured as PWM signal

5.2.2 Two-wire Interface (I2C Compatible)

The two-wire interface can communicate with a bi-directional wired-AND bus with two lines (SCL, SDA). The protocol makes it possible to interconnect up to 127 individually addressable devices. The interface is capable of clock stretching, supporting data rates of 100 kbps, 250kbps and 400 kbps. The module has 2 TWI ports and their properties like following table.

Instance	Master/Slave
TWI 0	Master
TWI 1	Master

5.2.3 Flash Program I/Os

The module has two programmer pins, respectively SWDCLK pin and SWDIO pin. The two pin Serial Wire Debug (SWD) interface provided as a part of the Debug Access Port (DAP) offers a flexible and powerful mechanism for non-intrusive debugging of program code. Breakpoints and single stepping are part of this support.

5.2.4 Serial Peripheral Interface

The SPI interfaces enable full duplex synchronous communication between devices. They support a three-wire (SCK, MISO, MOSI) bi-directional bus with fast data transfers. The SPI Master can communicate with multiple slaves using individual chip select signals for each of the slave devices attached to a bus. Control of chip select signals is left to the application through use of GPIO signals. SPI Master has double buffered I/O data. The SPI Slave includes EasyDMA for data transfer directly to and from RAM allowing Slave data transfers to occur while the CPU is IDLE. The GPIOs are used for each SPI interface line can be chosen from any GPIOs on the device and independently. This enables great flexibility in device pinout and efficient use of printed circuit board space and signal routing.

5.2.5 UARTs

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS), support in hardware up to 1 Mbps baud. Parity checking is supported. Support the following baudrate in bps unit:

1200/2400/4800/9600/14400/19200/28800/38400/57600/76800/115200.

- Note: The GPIOs are used for each SPI/TWI/UART interface line can be chosen from any GPIOs on the device and configed independently.

5.2.6 Analog to Digital Converter (ADC)

The 12 bit incremental Analog to Digital Converter (ADC) enables sampling of up to 8 external signals through a front-end multiplexer. The ADC has configurable input and reference prescaling, and sample resolution (8,10, and 12 bit).

- Note: The ADC module uses the same analog inputs as the LPCOMP module. Only one of the modules can be enabled at the same time.

MK04 Pin Number	Pin Number	Description
5	P0.28	Digital I/O; Analog input 4
6	P0.29	Digital I/O; Analog input 5
7	P0.30	Digital I/O; Analog input 6
8	P0.31	Digital I/O; Analog input 7
13	P0.02	Digital I/O; Analog input 0
14	P0.03	Digital I/O; Analog input 1
15	P0.04	Digital I/O; Analog input 2
16	P0.05	Digital I/O; Analog input 3

5.2.7 Low Power Comparator (LPCOMP)

In System ON, the block can generate separate events on rising and falling edges of a signal, or sample the current state of the pin as being above or below the threshold. The block can be configured to use any of the analog inputs on the device. Additionally, the low power comparator can be used as an analog wakeup source from System OFF or System ON. The comparator threshold can be programmed to a range of fractions of the supply voltage.

5.2.8 Reset

The reset pin of the MK04 module is in the internal pull-high state , when the reset pin of the module is input to a low level , the module will be automatically reset .After the reset pin is used , the parameters of the current setting will not be reserved .

5.2.9 NFC

The NFC peripheral (referred to as the 'NFC peripheral' from now on) supports communication signal interface type A and 106 kbps bit rate from the NFC Forum. With appropriate software, the NFC peripheral can be used to emulate the listening device NFC-A as specified by the NFC Forum.

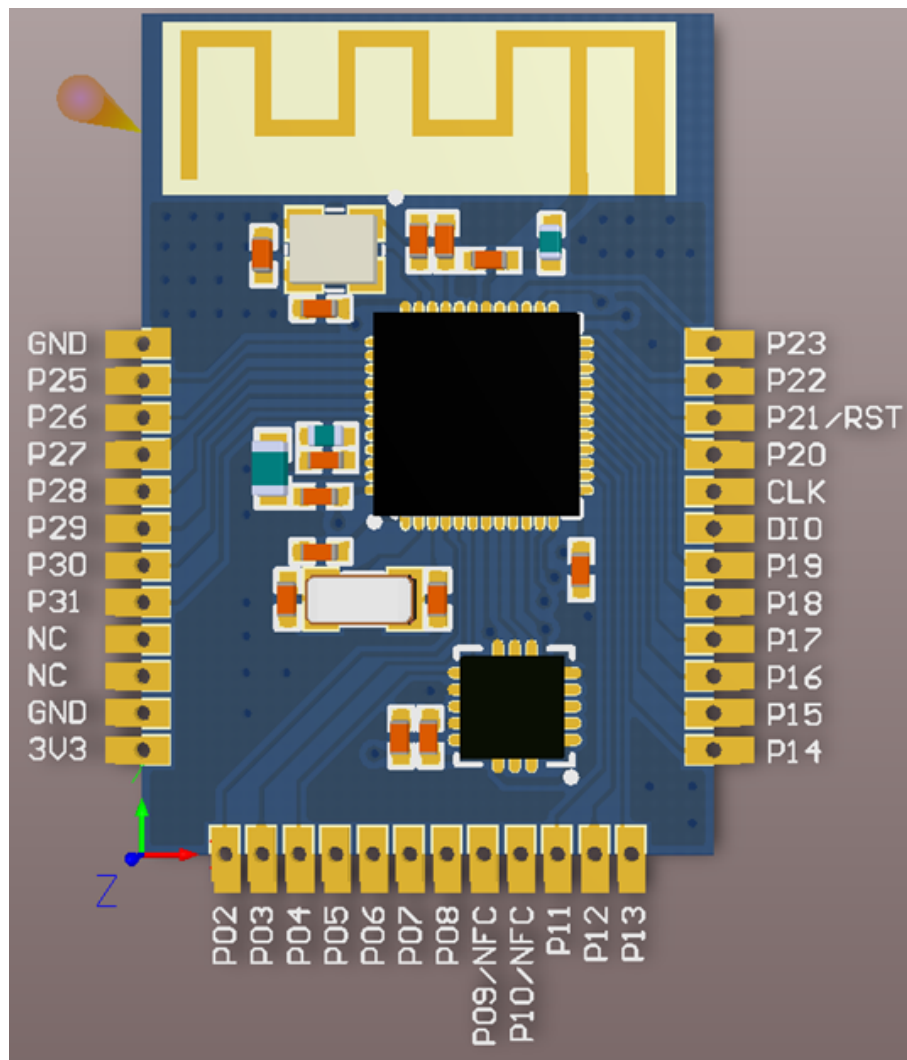
Listed here are the main features for the NFC peripheral:

- ◆NFC-A listen mode operation
- ◆13.56 MHz input frequency
- ◆Bit rate 106 kbps
- ◆Wake-on-field low power field detection (SENSE) mode
- ◆Frame assemble and disassemble for the NFC-A frames specified by the NFC Forum
- ◆Programmable frame timing controller
- ◆Integrated automatic collision resolution, CRC and parity functions

MK04 Pin Number	Pin Number	Description
20	P0.09	Digital I/O; NFC1
21	P0.10	Digital I/O; NFC2

6. Module Pinout and Pin Description

6.1 Module Pinout



6.2 Pin Description

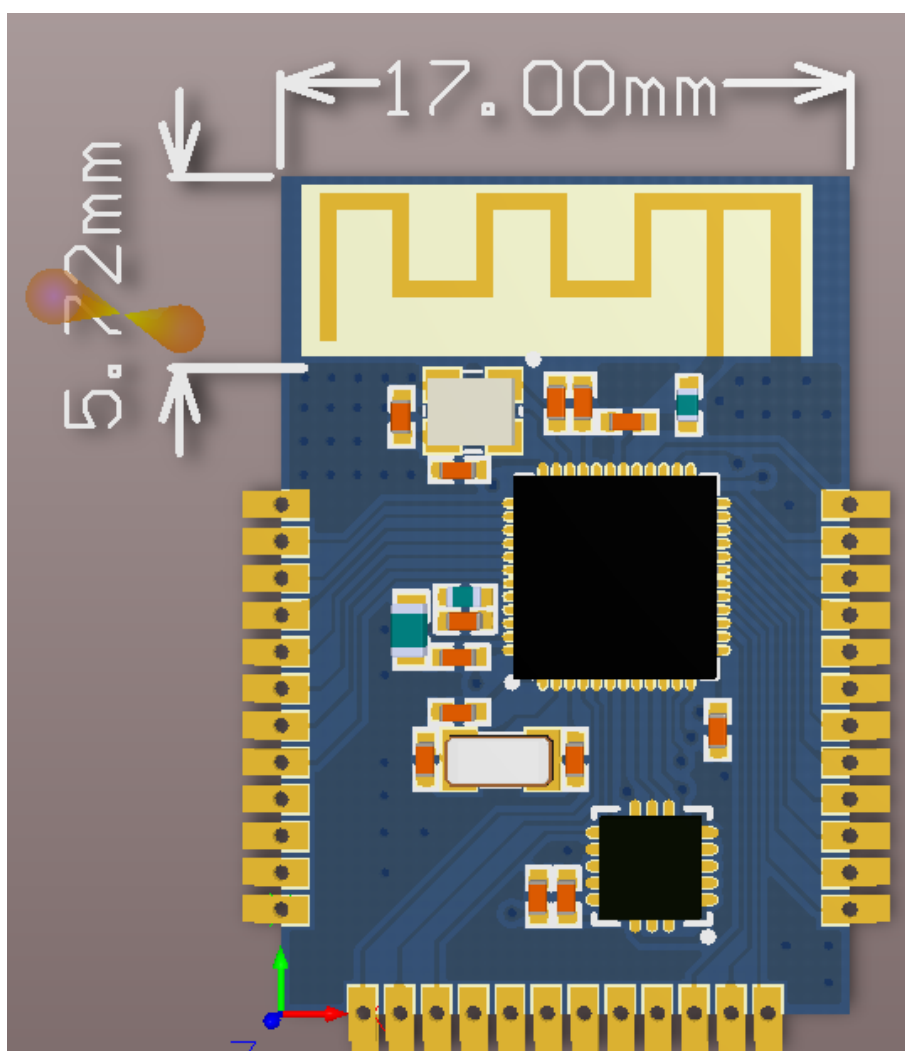
Pin NO.	Pin Name	Description	Remark
1	GND	Ground	-
2	P0.25	General Purpose I/O	Digital I/O
3	P0.26	General Purpose I/O	Digital I/O
4	P0.27	General Purpose I/O	Digital I/O
5	P0.28	Digital I/O; Analog input 4	SAADC/COMP/LPCOMP input

Pin NO.	Pin Name	Description	Remark
6	P0.29	Digital I/O; Analog input 5	SAADC/COMP/LPCOMP input
7	P0.30	Digital I/O; Analog input 6	SAADC/COMP/LPCOMP input
8	P0.31	Digital I/O; Analog input 7	SAADC/COMP/LPCOMP input
9	-	NC	-
10	-	NC	-
11	GND	Ground	-
12	VCC	Power Supply	1.8V-3.6V
13	P0.02	Digital I/O; Analog input 0	SAADC/COMP/LPCOMP input
14	P0.03	Digital I/O; Analog input 1	SAADC/COMP/LPCOMP input
15	P0.04	Digital I/O; Analog input 2	SAADC/COMP/LPCOMP input
16	P0.05	Digital I/O; Analog input 3	SAADC/COMP/LPCOMP input
17	P0.06	General Purpose I/O	Digital I/O
18	P0.07	General Purpose I/O	Digital I/O
19	P0.08	General Purpose I/O	Digital I/O
20	P0.09/NFC1	General Purpose I/O; NFC1	Digital I/O
21	P0.10/NFC2	General Purpose I/O; NFC2	Digital I/O
22	P0.11	General Purpose I/O	Digital I/O
23	P0.12	General Purpose I/O	Digital I/O
24	P0.13	General Purpose I/O	Digital I/O
25	P0.14	General Purpose I/O	Digital I/O
26	P0.15	General Purpose I/O	Digital I/O
27	P0.16	General Purpose I/O	Digital I/O
28	P0.17	General Purpose I/O	Digital I/O
29	P0.18	General Purpose I/O	Digital I/O
30	P0.19	General Purpose I/O	Digital I/O

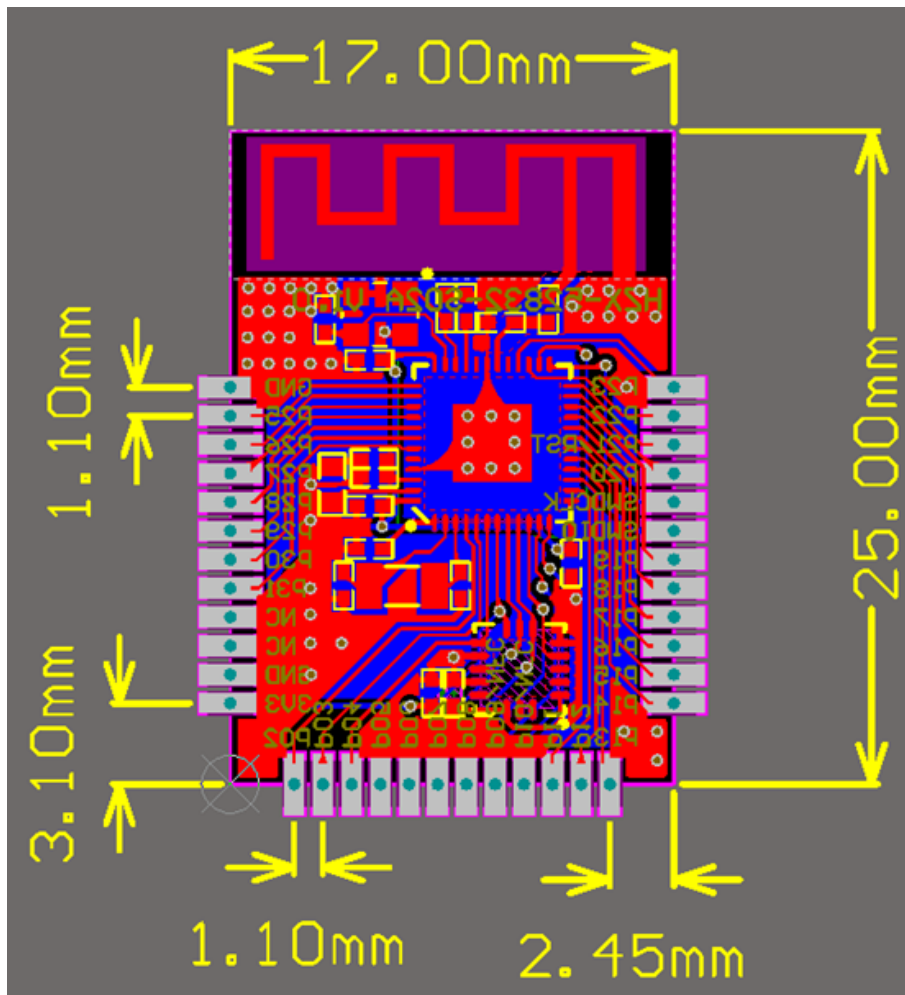
Pin NO.	Pin Name	Description	Remark
31	SWDIO	Digital I/O	Hardware Debug and Flash Program I/O
32	SWDCLK	Digital input	Hardware Debug and Flash Program I/O
33	P0.20	General Purpose I/O	Digital I/O
34	P0.21/RESET	General Purpose I/O; nRESET	Digital I/O
35	P0.22	General Purpose I/O	Digital I/O
36	P0.23	General Purpose I/O	Digital I/O

7. PCB Design Guide

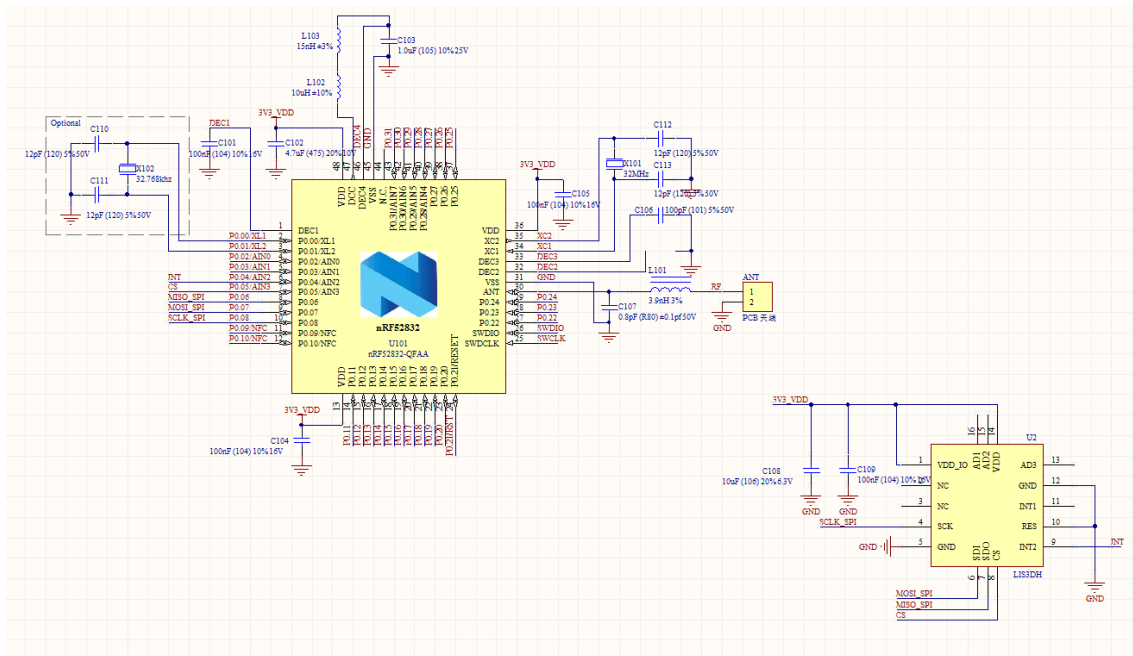
Please reserve empty area for PCB antenna when you are going to design a device' s board, the empty range minimum size : 17×5.72mm , please kindly check the picture below for reference.



8. PCB Footprint and Dimensions



9. Schematic



10. Declaration

The contents of this datasheet are subject to change without prior notice for further improvement. MOKO team reserves all the rights for the final explanation.

Please contact MOKO sales team or visit <http://www.mokosmart.com>

(<http://www.mokosmart.com>) to get more related information if needed.

Contact Information

MOKO TECHNOLOGY LTD.

Address : 4F,Buidling2, Guanghui Technology Park, MinQing Rd, Longhua, Shenzhen, Guangdong, China

Telephone : 86-75523573370

Fax : 86-75523573370-808

Website : <http://www.mokosmart.com> (<http://www.mokosmart.com>)

Revision History

Revision	Description of changes	Approved	Revision Date
V1.0	Initial Release	Kevin	2018.06
V1.1	Added product classification	Kevin	2018.07.18
v1.2	Modify Key Features and Applications	Kevin	2019.08.12

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